

# ABSTRACT OF THE DISCLOSURE

To achieve improved jitter performance within prescribed bandwidth constraints, a receiver (140) samples a digital signal (11) upon each of  $n$  periodic sample clock pulses that occur during the interval  $t$ , where  $n$  is chosen such that  $\log_2(n+1)$  is an integer ( $x$ ) greater than zero. At the each of each interval  $t$ , the receiver generates a  $x+1$ -bit sample value having a first bit indicating the value of the digital signal being sampled, and  $x$  remaining bits which collectively indicate a sample interval during which the digital signal changed states if such a change did occur. When a change does occur, the receiver inverts the first bit of each sample value upon decoding to coincide with the change in the digital signal.